**CHAPTER 1**

**INTRODUCTION**

**1.1 MOTIVATION**

Power reduction in SoC based embedded systems, is one of the important design specifications of VLSI design. This project deals with the reduction in power consumed by memory in SoC with acceptable trade off of stability and delay.

SoCs integrate multiple functions on a single silicon die. As process geometries have scaled, designs which use more and more of the additional silicon real estate available on chips to integrate embedded memories evolved. These embedded memories allow for significantly better system performance and lower power compared to a solution where off-chip memories are used. Most current designs have over 50% of their area used by embedded memories and these memories account for 50-70% of the total SoC power dissipation. Clearly, any attempt to reduce SoC power is incomplete if it does not attempt to reduce the power consumed by the embedded memories in the design.

Embedded cache memories are implemented using SRAM cells. SRAM is a type of [semiconductor](http://en.wikipedia.org/wiki/Semiconductor) memory that uses [bi-stable](http://en.wikipedia.org/wiki/Multivibrator) [latching circuitry](http://en.wikipedia.org/wiki/Flip-flop_(electronics)) to store each bit. A conventional SRAM has a 6T design. It is volatile in the conventional sense that data is eventually lost when the memory is not powered. So designing the SRAMs which consume less power becomes crucial. The cache is a smaller, faster memory which stores copies of the data from the most frequently used [main memory](http://en.wikipedia.org/wiki/Main_memory) locations. As long as most memory accesses are cached memory locations, the accesses time of memory will be closer to the accesses time of cache than to the access time of main memory. Hence improving the speed of cache becomes important.

**1.2 OBJECTIVE**

The objective of this project is to implement a cache memory using 4T SRAM and compare it with conventional 6T SRAM cache for parameters like power, delay and area, then implement buffered bit-line technique on 4T SRAM cache to get an optimized design with low power and lesser delay.